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FUNCTIONAL – THERMAL SIMULATION MODELS FOR DIGITAL INTEGRATED CIRCUITS

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The paper presents a mixed functional-thermal simulation model for gate level digital integrated circuits. It focuses on the thermal models implementation methods in digital simulation environments.

Key words: Verilog; thermal; simulation.

1. INTRODUCTION

Large digital circuits design requires more and more efficient algorithms for logic synthesis and place & route processes. In this context thermal phenomena become important and accurate estimation of temperature distribution leads to a better functional simulation.

Two important directions for improving functional simulation of digital integrated circuits are CAD tools improvement and models development. In post–layout simulations of large digital integrated circuits, temperature is a critical factor, usually estimated and modeled as a set of 3 predefined values: minimum, typical and maximum.

This paper describes the mixed functional and thermal modeling of digital circuits. By adding a "thermal" dimension in the simulation model, benefits can be obtained in terms of better functionality modeling and thermal behavior estimation. There are several ways for thermal behavior modeling. This paper presents two methods and focuses on the implementation of the discretized heat equation.

A direct application of mixed functional - thermal modeling is also presented. It describes the logic synthesis constraints based on the propagation delays measurement of the combinational paths in digital circuits.

Another aspect of mixed functional – thermal simulation of digital circuits is the actual simulation environment, based on the available simulators. Building such environments usually influences the simulation model itself and requires tradeoffs between the simulation accuracy and the simulation overhead.

Verilog [2] and VHDL are specialized, standardized hardware description languages intensively used in digital design. They are equally used in the industry and are almost equivalent at gate level circuit modeling. Verilog covers better both low level and system level modeling and, together with the PLI interface, is a fast and efficient solution for thermal net implementation. We chosen Verilog as the base language for both thermal model and simulation environment implementation.

2. SIMULATION MODEL

The thermal model of a digital integrated circuit can be implemented in several ways. The main constraints here come from the limitation of the specific simulation environments that are used in digital design.

The first approach solves the heat equation into a discretized space. This method is constrained by the limited mathematical capabilities of the Verilog/VHDL description languages and by the overhead introduced into simulation by the thermal model.

Equation 1 presents the simplified heat equation. It contains thermal generation and diffusion terms [1]. The thermal generation is based on the electrical energy dissipation from each device in the circuit. The thermal model is strongly linked to the functional model. In the particular case of CMOS digital circuits, power is consumed mainly at logic transitions. That is every logic transition of every component produces heat and contributes to the thermal model.

$$C_{th}\frac{dT}{dt} = p_{gen} + vp_{diff} = I_{average} * V - kA\frac{dT}{dx} \tag{1}$$

Equation 2 shows the 2D discretized form of the heat equation.

$$C_{th} * (T_{new} - T_{prev}) = P_{gen} - k * A * (\frac{T_{prev} - T_n}{d_y} + \frac{T_{prev} - T_s}{d_y} + \frac{T_{prev} - T_w}{d_x}\frac{T_{prev} - T_e}{d_y}) \tag{2}$$

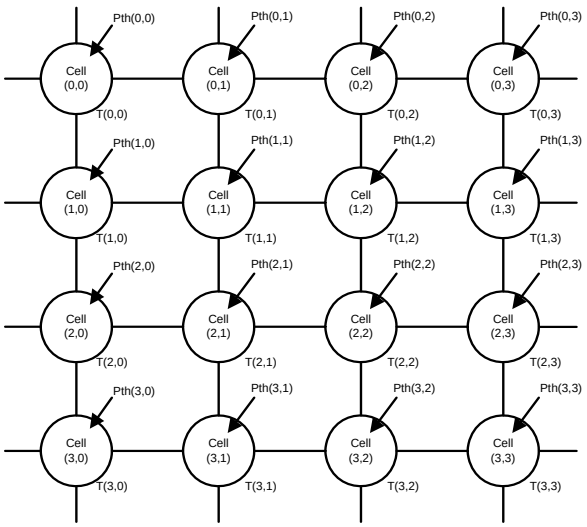

Figure 1 Thermal model implemented as a bi-dimensional net

where:

Cth - thermal capacitance

pgen - disipated power

vpdiff – diffusion generic term

Iaverage - average electrical current through the digital device

k - thermal conductivity

A – area unit

Tn,Tw,Ts,Te – respectively north neighbor cell, west neighbor cell, south neighbor cell, east neighbor cell temperature values.

The heat equation computation is performed in each discretization point of the thermal net, Figure 1. We called “thermal net” the implementation of the thermal model for the digital ICs.

Each digital component is dually modeled by the specific logic function and by its thermal model. Figure 3 describes the functionality of the 2 inputs AND gate with thermal capability and shows the interaction with the "thermal net". Basically it implements two additional functionalities:

- Models the propagation delay dependency of temperature. Temperature is continuously provided by the thermal net. Figure 2 presents the dependency obtained by successive SPICE simulations of a standard CMOS inverter.
- Collects the electrical power as energy quanta and provides it to the thermal net to used at the temperature distribution computation.

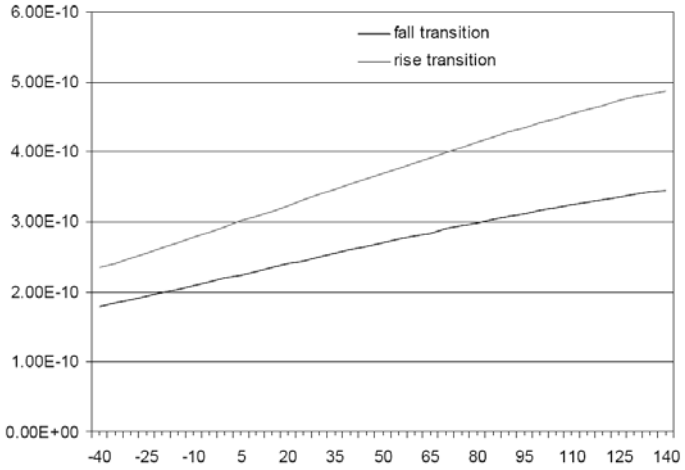

Figure 2 Propagation delay dependency upon temperature

The circuit generates heat and its temperature is increased; the thermal model receives the heat flows, computes the temperature distribution and provides the temperature values back to the circuit[4].

The implementation of Equation 1 is done in Verilog and C [6]; C code can be integrated into Verilog via PLI standardized interface[2]. Practical considerations dictate the model splitting in two components:

- Common model, implementing the heat equation and the actual thermal net.
- Circuit specific model that implements the thermal links between digital components and the thermal net.

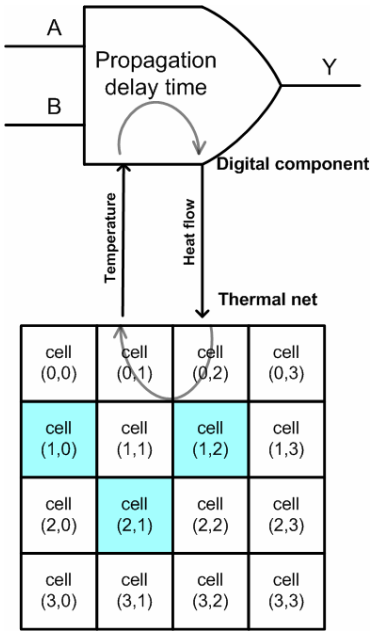

Figure 3 Digital components simulation models

An automated process was developed to create the models based on: circuit topology, geometric information and placement of the components [6].

The second way in creating a thermal model for integrated circuits uses the Electrical – Thermal analogy. This approach allows thermal effects to be modeled by electrical components such as resistors and capacitors. Table 1 lists some of the relevant electrical and thermal analogue quantities.

Table 1 Electrical and Thermal Analogue quantities

Electrical		Thermal	
Quantity	Unit	Quantity	Unit
Voltage V	V	Temperature T	K
Current I	A	Heat Flow q	W=J/s
Conductivity σ	I/V*cm	Conductivity k	W/K*cm
Electrical Charge Q	C	Heat H	J
Electrical Resistance R	V/A	Thermal Resistance Rth	K/W
Electrical Capacitance C	C/V	Thermal Capacitance Cth	J/K

The approach is suitable for transistor level description of the digital circuits. It can be implemented in SPICE like simulation environments.

3. **RESULTS**

This section presents an example of a mixed simulated circuit and proposes an application for thermal results. Figure 4 presents the schematic view of a circuit simulated in mixed functional – thermal environment

Each component resides into a certain position of the thermal net, according to the placement process, as depicted in Figure 6. The circuit has two logically identical buffers chains with outputs a and b entering into a XOR gate. The placement of the buffers chains and the flip-flops is in such manner that chain b area temperature gets higher that a.

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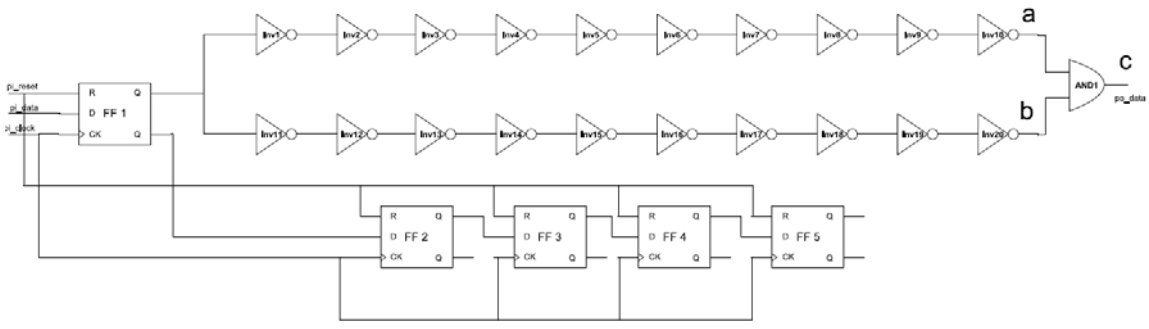

Figure 4 Digital circuit simulated in electro-thermal environment

Figure 6 shows the temperature distribution on the circuit area. As a consequence of this behavior the c pin has ‘1’ value spikes instead being all the time ‘0’. In classical simulations the a and b signals are identical during the entire simulation.

This example shows the ability of the model to extend the functional description beyond pure digital behavior. It is possible to simulate temporary malfunctions of the circuit caused by extensive heat.

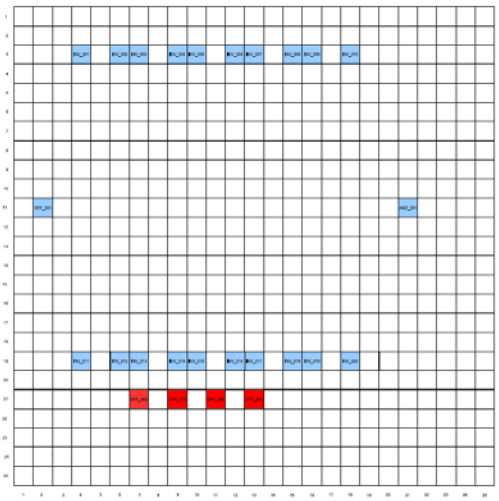

Figure 5 Placement information

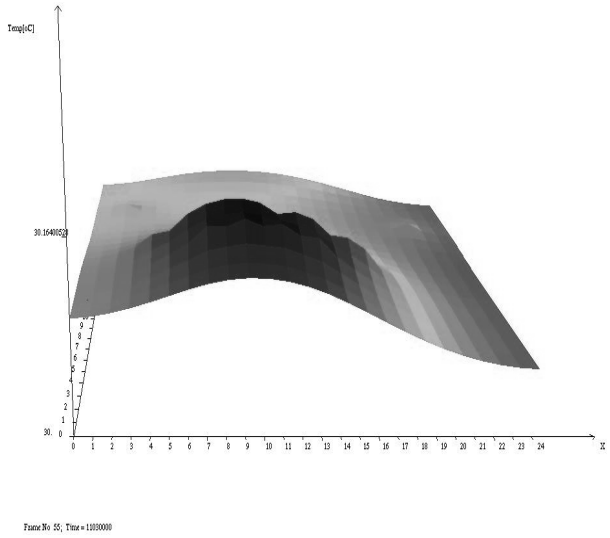

Figure 6 Temperature distribution over the thermal net

The thermal results of the electro-thermal simulation is a list of values from the thermal net containing propagation delay values for all the components and temperature values for all the net nodes; these values types are recorded during the simulation at consecutive moments. Figure 6 presents the 2D temperature distribution on chip for the circuit presented in Figure 8 as a result of the electro-thermal simulation

Figure 7 shows the evolution of the internal signals a and b as well as the output po_data from the described circuit. Due to the temperature evolution, the two nodes a and b become temporarily different so the output po_output takes non-zero values. Figure 8 presents the same circuit simulated without thermal model involved.

An interesting application uses the thermal simulation results to analyze the propagation delays through combinational paths improving digital synthesis process. The detected long paths can be further constrained to the desired value while short ones can be excluded from eventual existing constraints.

Another application of mixed simulation of large ICs provide the local areas temperature values upon a set of particular scenarios. By applying successive simulations, the resulting temperature distribution may be useful in Place and Route process as a set of constrains.

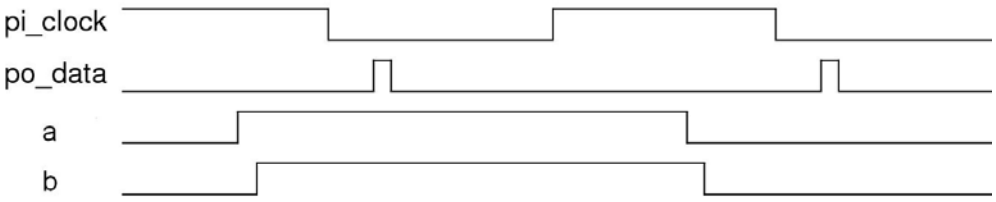

Figure 7 Digital signals values in case of mixed simulation

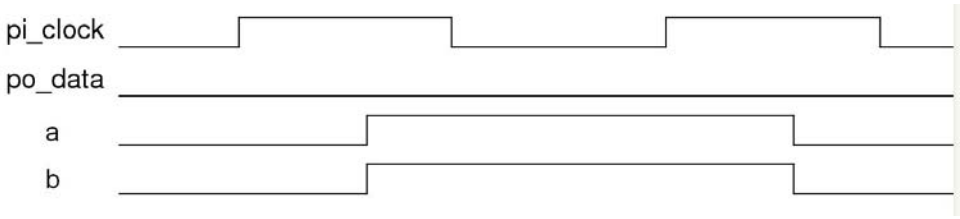

Figure 8 Digital signals values in case of classical digital simulation

4. CONCLUSIONS

The electro-thermal simulation environment links in the same simulation process two models of the same circuit: the functional one and the thermal behavior. The main advantages of the proposed simulation model in case of large integrated circuits are:

- Local and global temperature estimation on chip based on specific functionality scenarios. Different functional scenarios will lead to different thermal distributions.
- Better modeling of the digital circuit functional behavior; each component will adjust continuously its propagation delays based on local temperature value.

The main limitation of the model comes from its dependency on simulation scenario. Relevant simulation/verification scenarios should be created as different functions produce different temperature distributions.

The simulation environment closes the loop between the two phenomena; it is now possible to simulate timing violations together with their causes. The components propagation delays depend on the temperature which here is a simulation variable; functionality generates heat that may lead to some (temporary) timing violation of corresponding constraints. The electro-thermal simulation environment increases the simulation quality by adding the temperature dimension to the simulation.

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