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MEMORY PROPERTIES OF GE NANOCRYSTALS-BASED CAPACITORS WITH DIFFERENT COMPOSITION OF INTERMEDIATE LAYER

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Abstract. In this work, the charge storage properties of trilayers with Ge nanocrystals (NCs) embedded in HfO_2 matrix prepared by using two approaches for obtaining the intermediate layer with Ge NCs as nodes are investigated. Trilayer structures with tunnel and control oxides of HfO_2, but with different intermediate layers of Ge and Ge-HfO_2, respectively, were deposited by magnetron sputtering. Ge nanostructuring was achieved by subsequent rapid thermal annealing. Charge storage behaviour was studied by measurements of capacitance-voltage characteristics on MOS-like capacitors based on the annealed trilayers. The MOS samples with intermediate layer obtained by depositing a continuous Ge layer show hysteresis with memory windows up to ~1.3 V, while the ones with co-deposited Ge and HfO_2 as intermediate layer present higher memory windows, ~1.8 V. In both cases, the memory windows are independent on the frequency demonstrating that the memory effect is due to storing the charge only inside Ge NCs. These show that the approach based on co-deposition of a Ge-HfO_2 intermediate layer is more effective for charge storage with direct application in memory devices.

Key words: Ge nanocrystals, HfO_2, magnetron sputtering, rapid thermal annealing, charge storage properties

1. INTRODUCTION

Si and Ge nanocrystals (NCs) embedded in oxides have attracted high attention of the scientific community due to their applications in non-volatile memory devices, light emitters, and photodetectors [1, 2]. The importance of these nanostructured materials mainly comes from the size effect (limited by exciton Bohr radius) producing discrete quantum confinement energy levels in the widened band gap of NCs [3−8]. In these nanostructures, the electrical behaviour is mainly governed by tunnelling and hopping mechanisms [9−11]. The quantum confinement of carriers in NCs is used in different devices, in particular in non-volatile memories based on NCs in which the memory effect is produced by the storage of charge carriers in NCs. However, the properties of the nanostructured materials are strongly dependent on the presence of traps related to the quality of the NC/oxide matrix interface [12−15] and internal strains [16, 17]. It is known that traps influence the electrical properties [18, 19]. For example, the defects from the NC/oxide interface can also contribute to the memory effect [20]. Depending on the oxide matrix, the contribution of trap centres to the memory effect cannot be precisely controlled. These produce the partial stability in time of memories.

The Ge NCs in gate dielectric of SiO_2 were shown to have better performance than the Si NCs also embedded in SiO_2 [21] as the leakage current related to the direct tunnelling current is lower and the write voltage related to the onset voltage of Fowler-Nordheim tunnelling is reduced. MOS capacitors and MOSFETs based on Ge NCs in SiO_2 have been largely studied from the point of view of charge storage properties by analysing the effect of annealing time [22] and annealing temperature [23], tunnel oxide thickness [24], fast traps [25], and the number of Ge NCs layers in multilayers [26]. Non-volatile cross-bar memory structures with large number of memory cells based on SiO_2/Ge/SiO_2 on Si trilayers with Ge NCs embedded in the gate oxide with significant memory properties were fabricated [27].

Ge NCs in other oxides, e.g. HfO_2 [28, 29], $TaZrO_x$ [30], Al_2O_3 [31], HfAlO [32] are less studied. However, HfO_2 is a key dielectric, currently being used in flash memory devices instead of SiO_2 [33] as it has

high dielectric permittivity enabling a decreased equivalent oxide thickness that allows a more aggressive circuit scaling and presents asymmetric band offsets that favour an increased electron retention time.

In order to obtain good charge storage properties, the NC parameters related to density and position (separation distance between NCs and distance from substrate) have to be controlled. So, the formation of Ge NCs layer is crucial. It consists in the segregation of Ge in nanoparticles and their crystallization resulting in a layer formed of Ge NCs embedded in oxide matrix with good lateral separation. Usually, the Ge NCs formation is produced by controlling the annealing conditions (temperature, time, and atmosphere) [9, 34]. The charge retention is strongly dependent on the dielectric properties of oxide matrix and also on the spatial positioning of NCs between each other in oxide and from the substrate.

In this work, the memory properties of trilayers with Ge NCs embedded in HfO_2 matrix prepared by using two approaches for obtaining the intermediate layer with Ge NCs as nodes are investigated. For this, trilayer structures with tunnel and control oxides of HfO_2, but with different intermediate layers of continuous Ge and co-deposited Ge-HfO_2, respectively, are deposited by magnetron sputtering followed by Ge nanostructuring. The charge storage properties are evidenced by measuring capacitance-voltage ($C - V$) curves in the 100 kHz – 1 MHz interval. The results prove that the alternative approach based on co-depositing a Ge-HfO_2 intermediate layer is more effective for obtaining the highest memory windows.

2. SAMPLE PREPARATION AND MEASUREMENT TECHNIQUES

Ge NCs in HfO_2 matrix are obtained by making use of the trilayer approach consisting in deposition of HfO_2/(Ge or Ge-HfO_2)/HfO_2 trilayer structures on Si wafers [35]. First, (100) p-Si substrates of 7–14 Ωcm resistivity are cleaned in the cleanroom using standard recipes (wet chemical solution) and then the native Si oxide is removed by etching in diluted HF solution (2%). These substrates are immediately loaded in the magnetron sputtering equipment in which the pressure of 3×10^{-7} Torr is then achieved. Pure 6N Ar is flowed inside down to a working pressure of 4 mTorr. Three layers are successively deposited, first one (8–10 nm thickness) is tunnel oxide of HfO_2, the second one (4–10 nm thick) as intermediate layer of Ge or Ge-HfO_2, and the third one of control HfO_2 (20–25 nm thick). The top/control and bottom/tunnel HfO_2 layers are obtained by sputtering from HfO_2 target using 30–60 W RF power, while the intermediate layer is obtained by either sputtering Ge or co-sputtering Ge-HfO_2 using 5–15 W DC for Ge target and 30–40 W RF for HfO_2 target. So, HfO_2/(Ge or Ge-HfO_2)/HfO_2 trilayer structures on Si are obtained. All as-deposited samples are amorphous. So, in order to obtain Ge NCs in HfO_2, a rapid thermal annealing (RTA) is performed in the temperature interval of 600–650 ^oC for 4–8 min, in 6N-purity N_2 atmosphere. The investigated (annealed) samples denoted S1, S2, and S3 practically differ one from another by the intermediate layer. For S1, the as-deposited intermediate layer is a continuous Ge layer (4 nm thickness), while for S2 and S3, it was deposited by co-sputtering of Ge and HfO_2 (Ge to HfO_2 ratio is 2:1), for S2 being thinner (6 nm) than that (9 nm) for S3.

The charge storage behaviour was studied by measuring $C - V$ curves on MOS-like capacitors with 6.5×10^{-3} cm^2 Al contacts evaporated on top and backside of S1, S2, and S3 samples. The $C - V$ characteristics were recorded in dark at room temperature using an Agilent E4980A LCR meter. Their high frequency-behaviour was studied in the 100 kHz – 1 MHz interval. On the MOS-like capacitors, a postmetallisation annealing (PMA) was carried out in N_2 at 200–300 ^oC.

3. RESULTS AND DISCUSSION

In Fig. 1 are presented the normalized $C - V$ loops measured on sample S1 with RTA at 600 ^oC for 7 min. The used frequency is 1 MHz and the sweep voltages are (–3, +3), (–4, +4), and (–5, +5) V. The $C - V$ characteristics show counter-clockwise hysteresis demonstrating the injection of charges from the p-Si substrate into the NCs. From the sweep range dependence it results that the memory window increases with the widening of voltage sweep range reaching the highest value of about 1.3 V.

The frequency-behaviour of $C - V$ hysteresis loops was also studied, at three frequencies, 1 MHz, 500 kHz, and 100 KHz, in the (–5, +5) V range and the curves are given in Fig. 2. It is clear that the width of hysteresis (memory window) is independent on the frequency, meaning that the charge is stored only in Ge

NCs. In addition, a frequency-dependent shift of hysteresis is not observed, meaning that the contribution of fast traps from Ge NCs/matrix interface is negligible. One should take into account that the control capacitors prepared without Ge intermediate layer and annealed under similar conditions do not show any memory effect. This means that in the crystalline HfO_2 matrix, the slow traps that can act as charge storage nodes have low density and consequently their contribution to the memory effect is negligible [35]. Considering all these results, we can infer that the memory effect is produced by storing the charge only inside Ge NCs. Our previous morphology investigations [35] reveals that the trilayers with high density of Ge NCs and located at proper position have good charge storage properties.

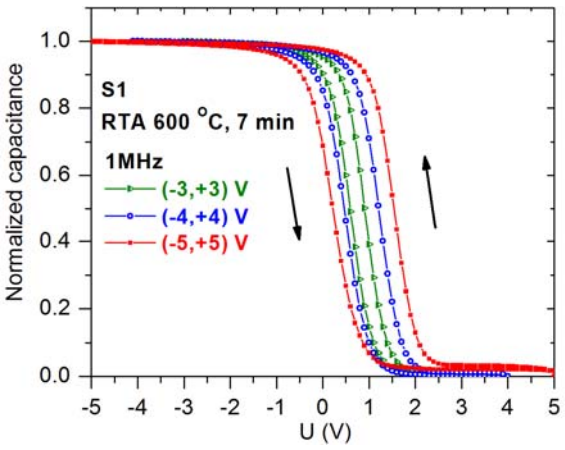

Fig. 1 – Normalized *C* – *V* loops measured on sample S1 with RTA at 600 °C for 7 min. The frequency is 1 MHz and the sweep voltages are (–3, +3), (–4, +4), and (–5, +5) V.

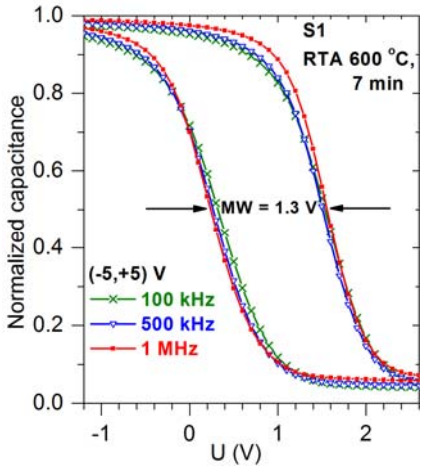

Fig. 2 – Normalized *C* – *V* hysteresis loops of capacitors S1 (RTA 600 °C, 7 min) measured at three frequencies, 1 MHz, 500 kHz, and 100 KHz. Sweep voltage is (–5, +5) V.

Figure 3 displays the normalized *C* – *V* curves measured at 1 MHz in the (–4,+4) V range on sample S2 with RTA at 600 °C for 7 min. One can see that capacitor S2 has negligible memory window meaning that a small density of NCs is formed in the thin co-deposited Ge-HfO_2 intermediate layer. Therefore, the Ge amount is too small, and consequently the density of Ge NCs is too low to have significant memory effect.

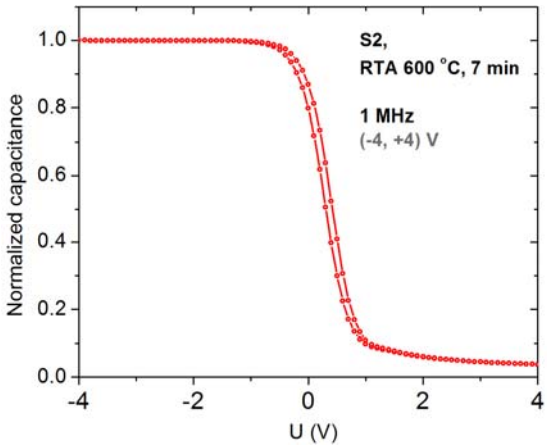

Fig. 3 Normalized *C* – *V* characteristics measured on sample S2 with RTA at 600 °C for 7 min. The frequency is 1 MHz and the sweep voltages is (–4, +4).

Considering the results obtained on sample S2 it is logical that the next step to be considered was to increase the Ge amount (sample S3 with increased thickness of co-deposited Ge-HfO_2 layer) and see the effect of it on the *C* – *V* loops. In Fig. 4, *C* – *V* curves recorded in the (–5, +8) V interval at the same frequencies (1 MHz, 500 kHz, and 100 KHz) on the capacitor S3 are shown. This capacitor was annealed under similar conditions as capacitors S1 and S2. Trilayer S3 also presents counter-clockwise *C* – *V* hysteresis, but with larger memory window (~1.8 V) than trilayer S1 (see Figs. 1 and 4).

Similarly with sample S1, the memory window is independent on frequency, i.e. the Ge NCs are the only charge storage nodes. In this trilayer, the as-deposited intermediate layer contains a bigger Ge amount (6 nm equivalent Ge thickness) than in S1 (4 nm Ge intermediate layer), so that it is logical to assume that the density of Ge NCs is higher in the trilayer S3. Sample S2 has the lowest Ge NCs density in the intermediate layer as the equivalent Ge thickness has 4 nm and the NCs are distributed in an intermediate layer of 6 nm thickness.

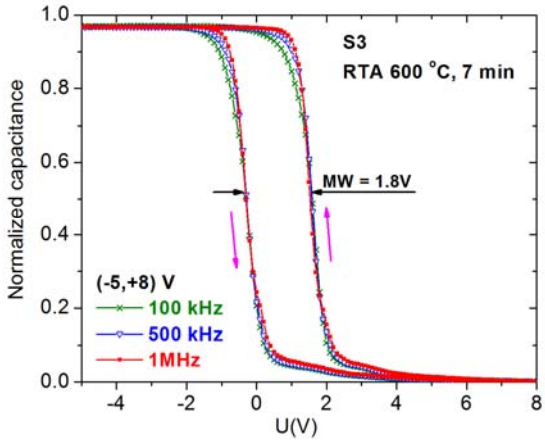

Fig. 4 Normalized *C* – *V* hysteresis loops of capacitors S3 (RTA 600 °C, 7 min) measured at three frequencies: 1 MHz, 500 kHz, and 100 KHz. Sweep voltage is (–5, +8) V.

Additionally, the intermediate layer deposited by co-sputtering of Ge and HfO_2 (and then annealed) contributes to obtaining by RTA of a good separation between Ge NCs.

4. CONCLUSIONS

The charge storage properties of trilayers with Ge NCs embedded in HfO_2 were studied by using two approaches for depositing the intermediate layer, one approach of depositing a continuous Ge layer and the other of co-depositing Ge and HfO_2. Three different capacitors were prepared, one with a continuous as-deposited Ge layer of 4 nm thickness (capacitor S1) and the other two (S2 and S3) with as-deposited intermediate layers of Ge-HfO_2 having different equivalent Ge thickness (4 nm for S2 and 6 nm for S3). This suggests that the highest Ge NCs density is found in trilayer S3, and the lowest density in S2. The *C* – *V* curves measured on the capacitors S1 and S3 present hysteresis with memory windows of 1.3 and 1.8 V, respectively.

The memory windows are independent on the frequency demonstrating the storing of charge inside Ge NCs, only. The largest memory window obtained for S3 proves that the highest density of Ge NCs corresponds to S3 trilayer, while the lowest memory window obtained on S2 demonstrates that the density of Ge NCs is the lowest. Also, the approach of trilayers with Ge-HfO_2 co-sputtered intermediate layer followed by RTA produces a good separation between Ge NCs. Consequently, the approach based on co-deposition of a Ge-HfO_2 intermediate layer is more effective for charge storage and has direct application for memory devices.

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