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NOVEL ASYMMETRIC/SYMMETRIC HALF-CASCADED MULTILEVEL INVERTER FOR PHOTOVOLTAIC BASED SHUNT ACTIVE POWER FILTER TO MITIGATE POWER QUALITY ISSUES

Amir KHANJANZADEH[1], Amin SOLEYMANI[2], Abdolhossein JOHARI[2]

[1] Department of Electrical Engineering, Chalus Branch, Islamic Azad University, Chalus, Iran
[2] Khuzestan Electric Power Distribution Company, Mahshahr, Iran
a.khanjanzadeh@iauc.ac.ir, amin.soleimani@kepdc.co.ir, abdjohari@kepdc.co.ir

Abstract. Photovoltaic (PV) technology has been recently developing and upgrading with regard to the rapid and high request from various agricultural, domestic and industrial electric power systems. Due to feasibility and reliability of Multi-Level Inverter (MLI), it can be effectively implemented in the photovoltaic systems. The large number of switches used in the MLIs is their main drawback which leads to lack of cost-effectiveness and high Total Harmonic Distortion (THD). In this paper, a novel Asymmetric/Symmetric Half-Cascaded MLI (ASHC-MLI) which contains low number of switches is proposed to attain a cost-effective structure. After that, PV panels have been used as power sources of this structure to construct the overall Shunt Hybrid Active Power Filter (SHAPF) for mitigating the power quality problems. To evaluate the cost-effectiveness of the proposed ASHC-MLI, it has been compared with the prominent and inventive MLI structures in both asymmetric and symmetric statuses. Meanwhile, the understudy power system has been affected by different current distortions so that the harmonic elimination capability of the proposed SHAPF can be well revealed. The evaluation analysis has been simultaneously performed for the conventional active power filter to appropriately validate its harmonic elimination capability.

Key words: photovoltaic, power quality, total harmonic distortion, Shunt Hybrid Active Power Filter, Asymmetric/Symmetric Half-Cascaded Multi-Level Inverter.

1. INTRODUCTION

The human need for any form of energy in various life aspects is inevitable which is considered as a basic principle for developed countries [1]. The energy shortages, rising greenhouse gases and ecological problems as major challenges have compelled the governments to more utilize new renewable energy. Among the renewable-based energy generation plants, solar energy as the most accessible, contamination-free and high-potential energy source is an excellent alternative instead of oil, gas and other fossil fuel sources to evade the climatic variations [2]. The most prominent problem is direct conversion of this energy into the electrical energy via PV system [3].

The PV system has been recently used as long-term DC power source of Flexible AC Transmission Systems (FACTS) devices such as Static Var Compensator (SVC), Static Compensator (STATCOM), Static Synchronous Series Compensator (SSSC), Dynamic Voltage Restorer (DVR) and Unified Power Flow Controller (UPFC) for different power system purposes. A new PV-STATCOM topology is proposed to stabilize the critical induction motor and enhance the fault ride-through capability [4]. The SVC has been integrated with PV system to additionally allow the reactive power control so that voltage drop/rise can be efficiently prevented [5]. Also, SSSC has been integrated with PV system to enhance the stable transmission constraints of power and voltage as well as damping control of PV-SSSC [6]. A special inter-harmonic control strategy is proposed for PV-UPFC to improve the sturdy force limitations and control the reactive power of the interconnected transmission system [7]. An AC-voltage synthesizer based on multilevel inverter is proposed for PV-DVR to compensate the balanced/unbalanced voltage sag and swell [8].

The maximum power of solar energy should be extracted under different weather conditions. In this regard, there are various strategies for maximum power point tracking (MPPT) for PV panels. These PV systems are basically designed based on two-stage energy conversion modes. The boost converter is mainly used in the first stage to track the MPP and increase the PV output voltage to a desired value. And then, the augmented DC voltage has been converted into the quasi-sinusoidal voltage/current using inverter for required voltage/current compensation purposes [9]. However, the PV-based DC voltage source due to its long-term energy generation can be integrated with battery energy storage to achieve a stable and continuous DC voltage source.

The power system includes many nonlinear devices such as power electronic converters, controllable speed drives, electric arc furnaces, etc., which present many different power quality issues related to current harmonics [10]. Active power filter is a compensator based on power electronics that absorbs the harmonic currents in the power system caused by the aforementioned nonlinear devices. Its performance is highly dependent on the structure of the inverter [11]. Since this compensator is commonly used in medium voltage systems, the conventional two/three-level inverters cannot properly perform the compensation process. Therefore, MLIs have been used in the APF structures to get rid of this problem. Multi-level inverters have several advantages as compared to the conventional two/three-level inverters. For instance, MLI-based APF can effectively decrease the harmonics components with increase of MLI levels, and also improve the power quality of output voltage [12]. The cascaded type of MLI had been firstly used in the motor drive structures [13], and afterward used to control the reactive power and compensate the harmonic components [14]. Due to the inherent balancing nature of the cascade inverters, they have appropriately operated in active filter structures. However, the voltage balances can slightly change due to the loss of circuit components and the complexity of the control system [15]. Apart from the mentioned advantages of MLIs, their critical problem is the need for multiple power electronic switches with corresponding gate drive circuits. This can complicate the inverter structure which makes it more expensive.

In the last decade, many different reduced MLI structures have been proposed to overcome this problem. Some of these MLI structures have been proficient to solve the quality of output quasi-sinusoidal voltage and their total cost-price. Moving towards these recent developments, this paper aims to propose a new MLI structure based on Asymmetric/Symmetric Half-Cascaded. Its unique and flexible structure along with asymmetric power supplies can make this inverter more competent to increase the number of voltage levels with low number of switches. To evaluate the voltage quality of the proposed ASHC-MLI and its cost-effectiveness, it has been compared with the prominent and inventive MLI structures in both asymmetric and symmetric statuses.

Subsequently, ASHC-MLI has been embedded in SHAPF to accurately diminish the current harmonics. In this regard, different current distortions have been considered for the understudy power system so that the harmonic elimination capability of the proposed SHAPF can be well revealed. The evaluation analysis has been simultaneously performed for the conventional active power filter to appropriately validate its harmonic elimination capability. Finally, the simulation results have transparently confirmed that the proposed ASHC-MLI-based SHAPF can provide the lowest current harmonic components as compared to the conventional active power filter.

2. DESIGN AND ANALYSIS OF DC POWER SUPPLY OF SHUNT ACTIVE POWER FILTER

As shown in Fig. 1, the SHAPF model is connected to the power system via the interface inductor along with the proposed ASHC-MLI structure. The current reference signal is produced to control the harmonic elimination process of SHAPF. Its DC-link voltage has been adjusted by a PI controller. Each voltage of PV panel has been augmented by a boost converter to feed the required DC voltage for each module of ASHC-MLI, and then connected to the power system via an interface inductor. The battery power storage system has adjusted the DC-link voltage via bidirectionally exchange power. That is to say, the battery storage system can be charged by extra energy of PV system, and accordingly this energy can be released during low solar energy. Also, a nonlinear load is used to create harmonic currents in the power system.

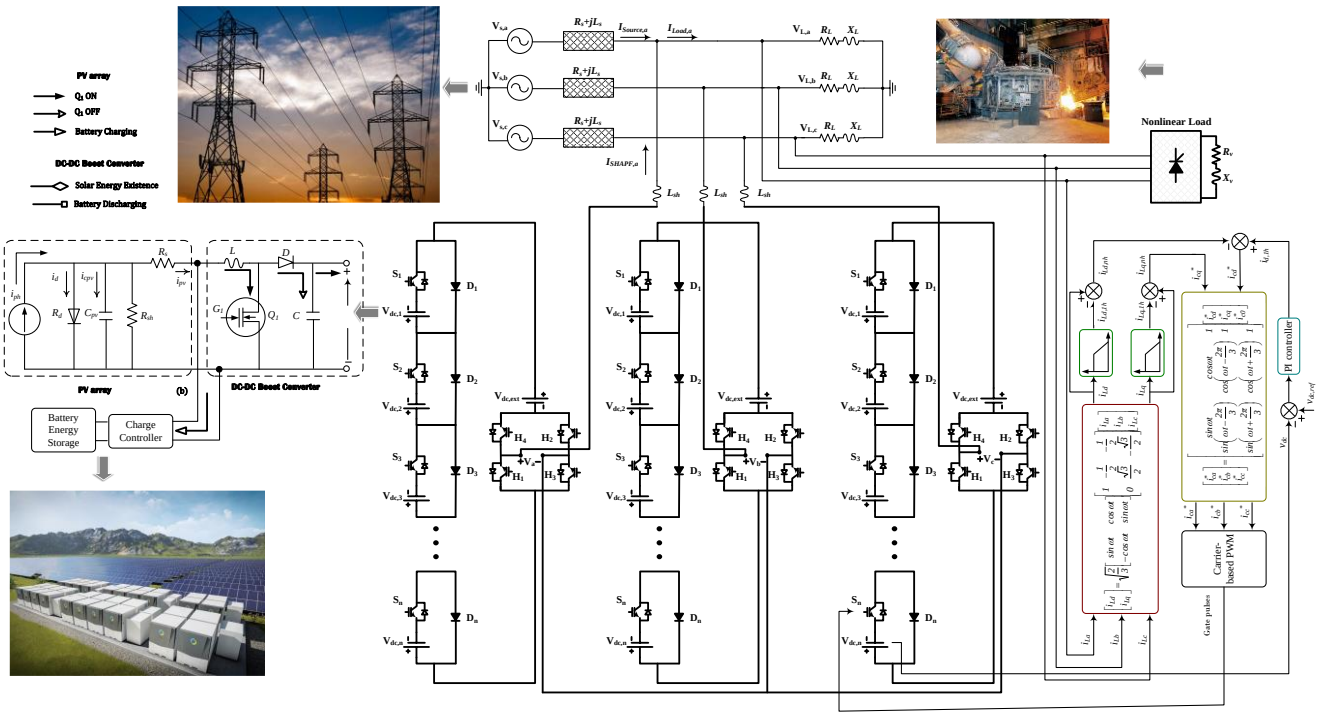


Fig. 1 – The power system with presence of proposed ASHC-MLI based SHAPF.

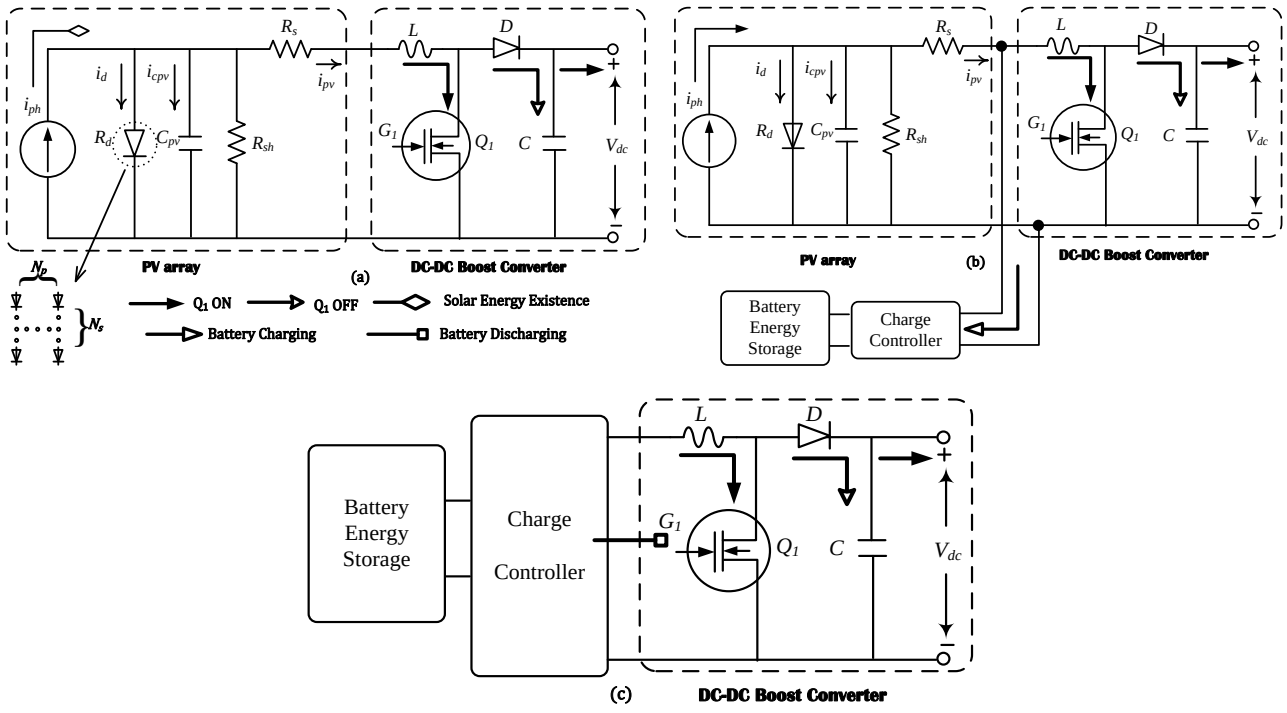


Fig. 2 – The PV current flow under three different operation conditions.

The PV system has been worked in three following conditions.

Condition 1. DC-links of ASHC-MLI have been fed to eliminate the current harmonics and compensate the reactive power. Its current flow path is presented in Fig. 2a.

Condition 2. This condition not only feeds the DC-links of ASHC-MLI, but also charges the battery energy storage from extra energy of the PV system. Its current flow path is presented in Fig. 2b.

Condition 3. The battery energy storage has provided the required DC voltage for DC-links of ASHC-MLI to eliminate the current harmonics and control the reactive power in cloudy times and no sunlight at night. Its current flow path is presented in Fig. 2c.

3. DESIGN AND COMPARISON OF ASYMMETRIC/SYMMETRIC HALF-CASCADED MULTILEVEL INVERTER

This paper proposes a new multilevel structure which is presented in Fig. 3. Each sub-multilevel part contains one DC source, one power electronic switch and one diode. All sub-multilevel parts have been cascaded to provide positive level creator. To complete the quasi-sinusoidal voltage, i.e., zero, positive and negative levels, an H-bridge is connected to the level creator part. This inverter can flexibly operate in both symmetric and asymmetric statuses. Both statuses have been thoroughly explained as follows.

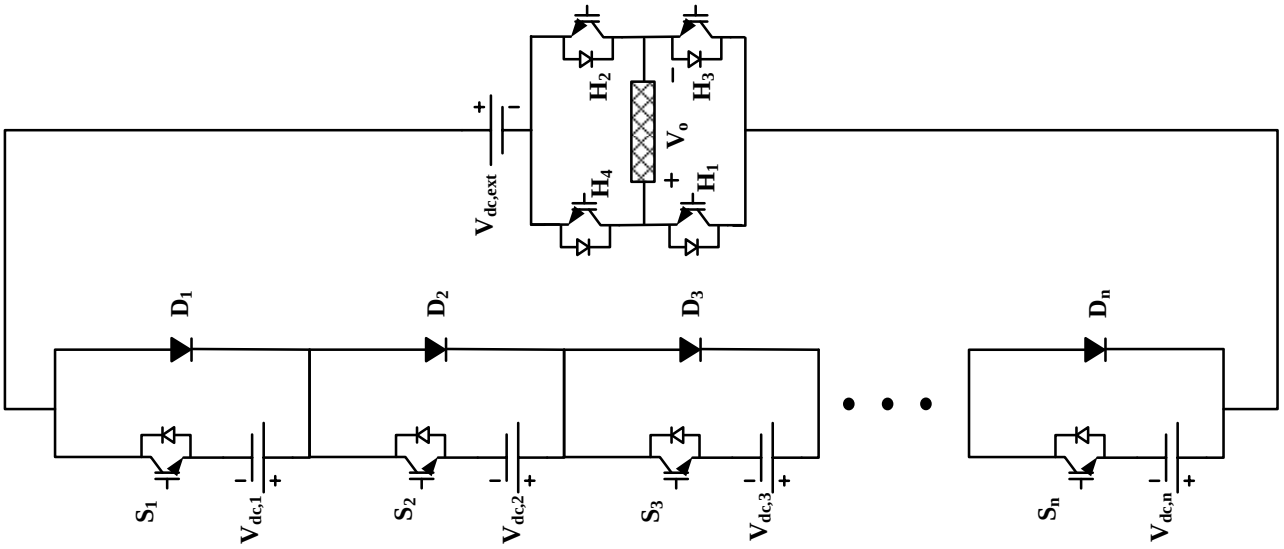


Fig. 3 – General structure of asymmetric/symmetric half-cascaded multilevel inverter.

According to Fig. 3, each sub-multilevel part contains only one unidirectional switch, whereas each sub-multilevel part of other MLIs has been structured by more than two switches (with considering two switches for bidirectional). Number of switches and diodes used in the proposed inverter is presented as follows in this structure can be calculated by:

$$N_{\text{switch}} = N_{source} + 3 \tag{1}$$

$$N_{\text{diode}} = N_{source} \tag{2}$$

Since the price of diode is very lower than power electronic switch as to the absence of gate driver circuit, protection circuit and suchlike, it has been discarded from the semiconductor count.

Indeed, its unique and flexible structure along with special progress for DC sources makes it more competent to increase the number of voltage levels with low number of switches. It has been compared with other prominent and inventive inverters in both asymmetric and symmetric statuses to validate its level-generation capability.

3.1. Symmetric operation mode

All DC sources are equal when ASHC-MLI operates in symmetric mode. To create quasi-sinusoidal voltage with low THD (high level), number of sub-multilevel parts must be increased. Each of them has provided one-positive level that all have been summed to provide final output voltage for level-creator part:

$$V_{\text{level-creator}} = \sum_{i=1}^{N_{\text{switch}}} V_i + V_d \tag{3}$$

With considering the value of V_d for all DC sources, number of voltage level for level-creator part can be presented as follows:

$$N_{\text{level-creator}} = N_{\text{switch}} + 1 \tag{4}$$

Then, an H-bridge is connected to the level creator part to complete the quasi-sinusoidal voltage. The total number of voltage level in symmetric mode can be presented as follows:

$$N_{\text{total-symmetric}} = 2\left(N_{\text{level-creator}} - 5\right) + 3 = 2N_{\text{switch}} - 5 \tag{5}$$

To confirm the voltage level creation of proposed inverter in this mode, four sub-MLIs are considered for proposed inverter which totally contains 8 switch and produces $2 \cdot 8 - 5 = 11$ levels. Table 1 presents switching operating sates of proposed inverter. Also, its relevant output voltages are presented in Fig. 4.

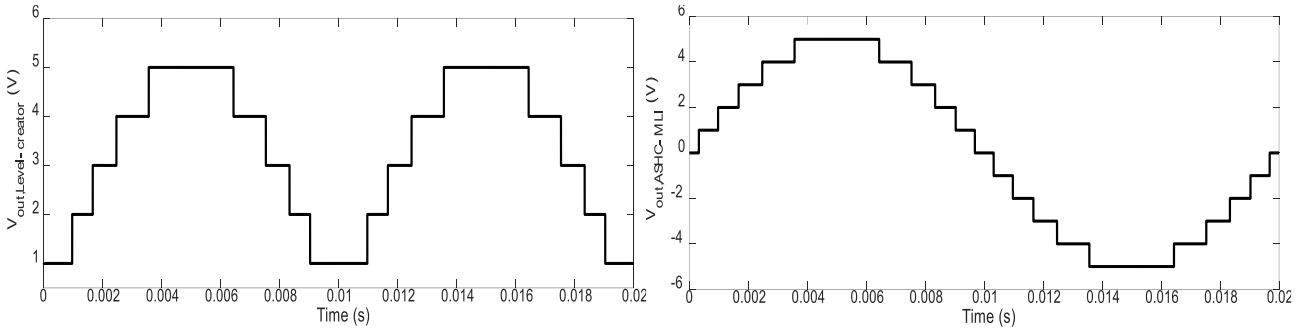


Fig. 4 – Output voltages of proposed multilevel inverter considering 11-level state.

Table1

The switching operating sates of the proposed inverter considering 11-level state

ON Semiconductors	$V_{\text{out\_symmetric}}$	ON Semiconductors	$V_{\text{out\_symmetric}}$
D_1, D_2, D_3, D_4, H_1, H_2	1	D_1, D_2, D_3, D_4, H_3, H_4	–1
S_1, D_2, D_3, D_4, H_1, H_2	2	S_1, D_2, D_3, D_4, H_3, H_4	–2
S_1, S_2, D_3, D_4, H_1, H_2	3	S_1, S_2, D_3, D_4, H_3, H_4	–3
S_1, S_2, S_3, D_4, H_1, H_2	4	S_1, S_2, S_3, D_4, H_3, H_4	–4
S_1, S_2, S_3, S_4, H_1, H_2	5	S_1, S_2, S_3, S_4, H_3, H_4	–5
H_1, H_3	0^+	H_2, H_4	0^-

3.2. Asymmetric operation mode

The asymmetric operation mode is used to increase the level count of output voltage without increase of the switch count. In this regard, the value of DC sources must be unequal and to be elected based on special progress. DC sources of the proposed ASHC-MLI are elected based on Binary progress. Hence, not only the level count of output voltage is increased (low THD), but also a cost-effective structure is provided. The sub-multilevel parts have been cascaded with each other to create semi-positive quasi-sinusoidal voltage. The final output voltage of level-creator part can be presented as follows:

$$V_{\text{level-creator}} = \sum_{i=1}^{N_{\text{switch}}} \left(2^i + 1\right) V_d \tag{6}$$

With considering binary progress for DC sources, number of the voltage level for level-creator part can be presented as follows:

$$N_{\text{level-creator}} = 2^{(N_{\text{switch}}-4)} \tag{7}$$

In the same way, H-bridge undertakes the completeness of the quasi-sinusoidal voltage. The total number of voltage level in asymmetric mode can be presented as follows:

$$N_{\text{total-asymmetric}} = 2\left(2^{N_{\text{switch}}-4}\right)+1 = 2^{(N_{\text{switch}}-3)}+1 \tag{8}$$

To confirm the voltage level creation of proposed inverter in this mode, four sub-MLIs are considered for proposed inverter which totally contains 8 switch and produces $2^{(8-3)}+1=33$ levels. Table 2 presents switching operating sates of proposed inverter. Also, its relevant output voltages are presented in Fig. 5.

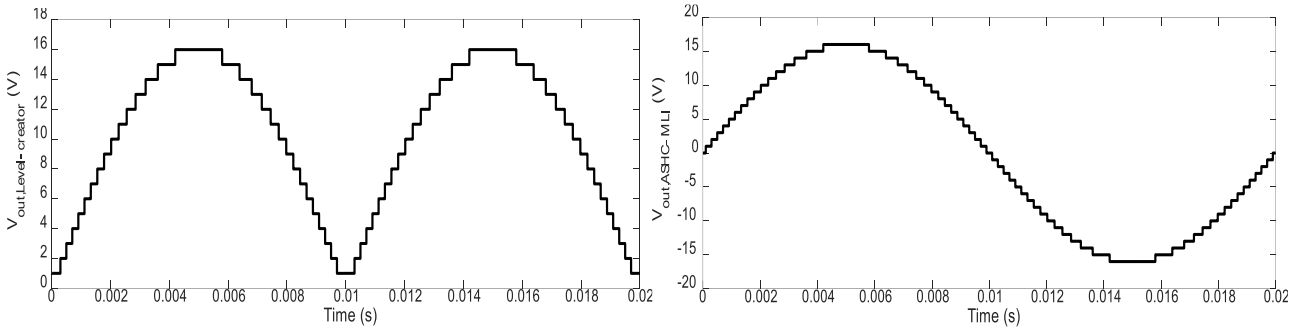


Fig. 5 – Output voltages of proposed multilevel inverter considering 33-level state.

Table2

The switching operating sates of the proposed inverter considering 33-level state

ON Switches	$V_{out\_symmetric}$	ON Switches	$V_{out\_symmetric}$
$D_1, D_2, D_3, D_4, H_1, H_2$	1	$D_1, D_2, D_3, D_4, H_3, H_4$	–1
$S_1, D_2, D_3, D_4, H_1, H_2$	2	$S_1, D_2, D_3, D_4, H_3, H_4$	–2
$D_1, S_2, D_3, D_4, H_1, H_2$	3	$D_1, S_2, D_3, D_4, H_3, H_4$	–3
$S_1, S_2, D_3, D_4, H_1, H_2$	4	$S_1, S_2, D_3, D_4, H_3, H_4$	–4
$D_1, D_2, S_3, D_4, H_1, H_2$	5	$D_1, D_2, S_3, D_4, H_3, H_4$	–5
$S_1, D_2, S_3, D_4, H_1, H_2$	6	$S_1, D_2, S_3, D_4, H_3, H_4$	–6
$D_1, S_2, S_3, D_4, H_1, H_2$	7	$D_1, S_2, S_3, D_4, H_3, H_4$	–7
$S_1, S_2, S_3, D_4, H_1, H_2$	8	$S_1, S_2, S_3, D_4, H_3, H_4$	–8
$D_1, D_2, D_3, S_4, H_1, H_2$	9	$D_1, D_2, D_3, S_4, H_3, H_4$	–9
$S_1, D_2, D_3, S_4, H_1, H_2$	10	$S_1, D_2, D_3, S_4, H_3, H_4$	–10
$D_1, S_2, D_3, S_4, H_1, H_2$	11	$D_1, S_2, D_3, S_4, H_3, H_4$	–11
$S_1, S_2, D_3, S_4, H_1, H_2$	12	$S_1, S_2, D_3, S_4, H_3, H_4$	–12
$D_1, D_2, S_3, S_4, H_1, H_2$	13	$D_1, D_2, S_3, S_4, H_3, H_4$	–13
$S_1, D_2, S_3, S_4, H_1, H_2$	14	$S_1, D_2, S_3, S_4, H_3, H_4$	–14
$D_1, S_2, S_3, S_4, H_1, H_2$	15	$D_1, S_2, S_3, S_4, H_3, H_4$	–15
$S_1, S_2, S_3, S_4, H_1, H_2$	16	$S_1, S_2, S_3, S_4, H_3, H_4$	–16
H_1, H_3	0^+	H_2, H_4	0^-

3.3. Comparison analysis and validation

The level-generation capability of the ASHC-MLI has been compared with other prominent and inventive inverters in both asymmetric and symmetric statuses in terms of switch count. In this regard, the proposed inverter has been distinctly compared in symmetric and asymmetric conditions.

Symmetric condition: The switch count equations in terms of voltage level count in the CHB inverter, CHB, [16], [17], [18] and [19] are presented as follows:

$$N_{\text{switch,[CHB]}} = 2\left(N_{\text{level}} - 1\right) \tag{9}$$

$$N_{\text{switch,[16]}} = \left(N_{\text{level}} + 3\right) \tag{10}$$

$$N_{\text{switch,[17]}} = \frac{3}{2}\left(N_{\text{level}} - 1\right) \tag{11}$$

$$N_{\text{switch,[18]}} = \frac{3}{2}\left(N_{\text{level}} - 1\right) \tag{12}$$

$$N_{\text{switch,[19]}} = \left(N_{\text{level}} + 1\right) \tag{13}$$

Asymmetric condition: in the same way, the switch count equations in terms of voltage level count in the binary, trinary, [20], [21], [22] and [23] are presented as follows:

$$N_{\text{Switch,binary}} = 4\frac{\ln\left(M_{\text{Level}} + 1\right)}{\ln 2} - 4 \tag{14}$$

$$N_{\text{Switch,trinary}} = 4\frac{\ln\left(M_{\text{Level}}\right)}{\ln 3} \tag{15}$$

$$N_{\text{Switch,ref[20]}} = 2\left(\frac{1}{3}M_{\text{Level}} - \frac{1}{9}\right)^{1/2} + \frac{23}{3} \tag{16}$$

$$N_{\text{Switch,ref[21]}} = 2\frac{\ln\left(M_{\text{Level}} - 6\right)}{\ln 2} + 4 \tag{17}$$

$$N_{\text{Switch,ref[22]}} = 3\frac{\ln\left(M_{\text{Level}} + 1\right)}{\ln 2} - 2 \tag{18}$$

$$N_{\text{Switch,ref[23]}} = \frac{5}{24}\left(M_{\text{Level}} + 15\right) + 4 \tag{19}$$

The comparison results in both the symmetric and asymmetric conditions are respectively presented in Fig. 6a and Fig. 6b. As can be seen, ASHC-MLI has presented an excellent level-generation capability than other prominent and inventive inverters in both asymmetric and symmetric conditions.

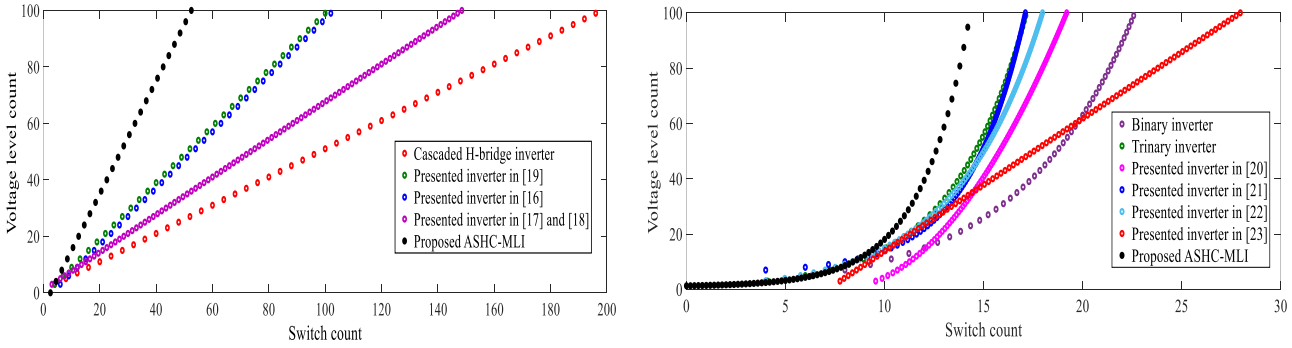
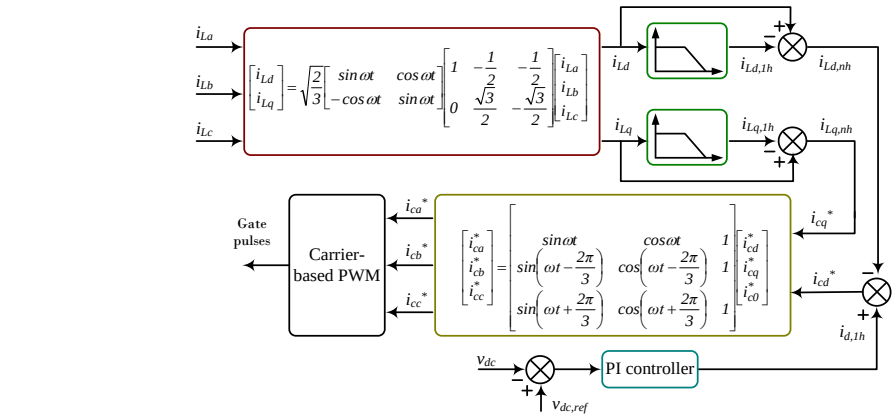


Fig. 6 – Voltage level count in terms of switch count in: a) symmetric condition; b) asymmetric condition.

4. DESIGN AND DESCRIPTION OF SHUNT HYBRID ACTIVE POWER FILTER

The general gate pulse generation control system and its simulation model are respectively presented in Fig. 7a and Fig. 7b. The d-q axis load currents (i_{Ld}, i_{Lq}) can be attained from three-phase instantaneous load currents (i_{La} , i_{Lb} , i_{Lc}) using Park transformation. The three-phase compensation current references (i_{ca}^* , i_{cb}^* and i_{cc}^*) have been used in carrier-based PWM process to provide switching signals for IGBT gates of the proposed multilevel inverter. Also, PI controller is used to eliminate the steady-state error due to existence of DC component in the reference signal.

The active and reactive parts can be decoupled in d-q load currents. i_{Ld} and i_{Lq} include both DC and AC terms. i_{d1h} indicates the fundamental frequency component of i_d for preserving the voltage balance of DC-link, and also compensating the internal power losses of the proposed shunt active power filter. Due to existence of DC component in the reference signal, PI controller is used to eliminate the steady-state error. In this regard, the deviation of V_{dc} and $V_{dc,ref}$ is entered into this controller that its output provide $i_{d,1h}$. The zero-sequence reference of the compensation current which is given in this figure has made the transformation matrix square one. Hence, $i_{c0}^* = 0$.



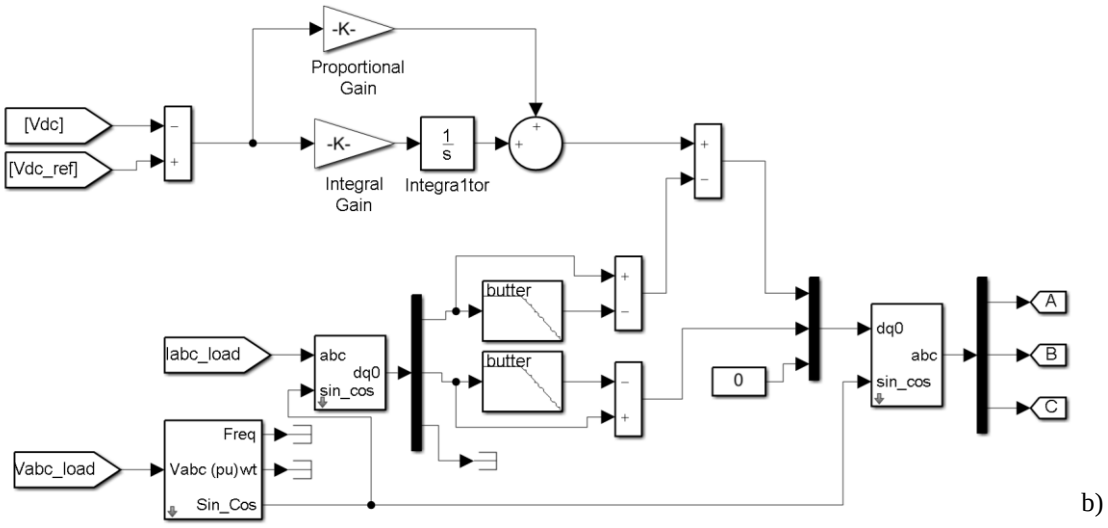


Fig. 7 – The general gate pulse generation strategy: a) block diagram model; b) MATLAB Simulink model.

5. SIMULATION RESULTS AND DISCUSSION

As mentioned before, this paper proposes ASHC-MLI to provide an accurate compensation current for reduction of the current harmonic caused by nonlinear loads, because it can provide high-level quasi-sinusoidal voltage as compared to the other structures. To evaluate the harmonic elimination capability of the proposed SHAPF, different current distortion conditions are considered. Since the proposed ASHC-MLI

contains twelve switches to provide 17-level quasi-sinusoidal voltage, same switches are considered for these understudy inverters so that an accurate comparison to be presented. The CHB, [16], [17], [18] and [19] can respectively provide 7, 9, 9, 9 and 11 levels. Hence, Ref. [19] due to provision of more level than other structures is considered for comparison study (as conventional inverter). The following sections' results have proved harmonic compensation capability of the proposed active filter. Meanwhile, the nominal parameters of three-phase rectifier and three-phase electric arc furnace loads and PV panel are provided in Table 3. Also, the furnace and rectifier load models have been provided in Fig. 8.

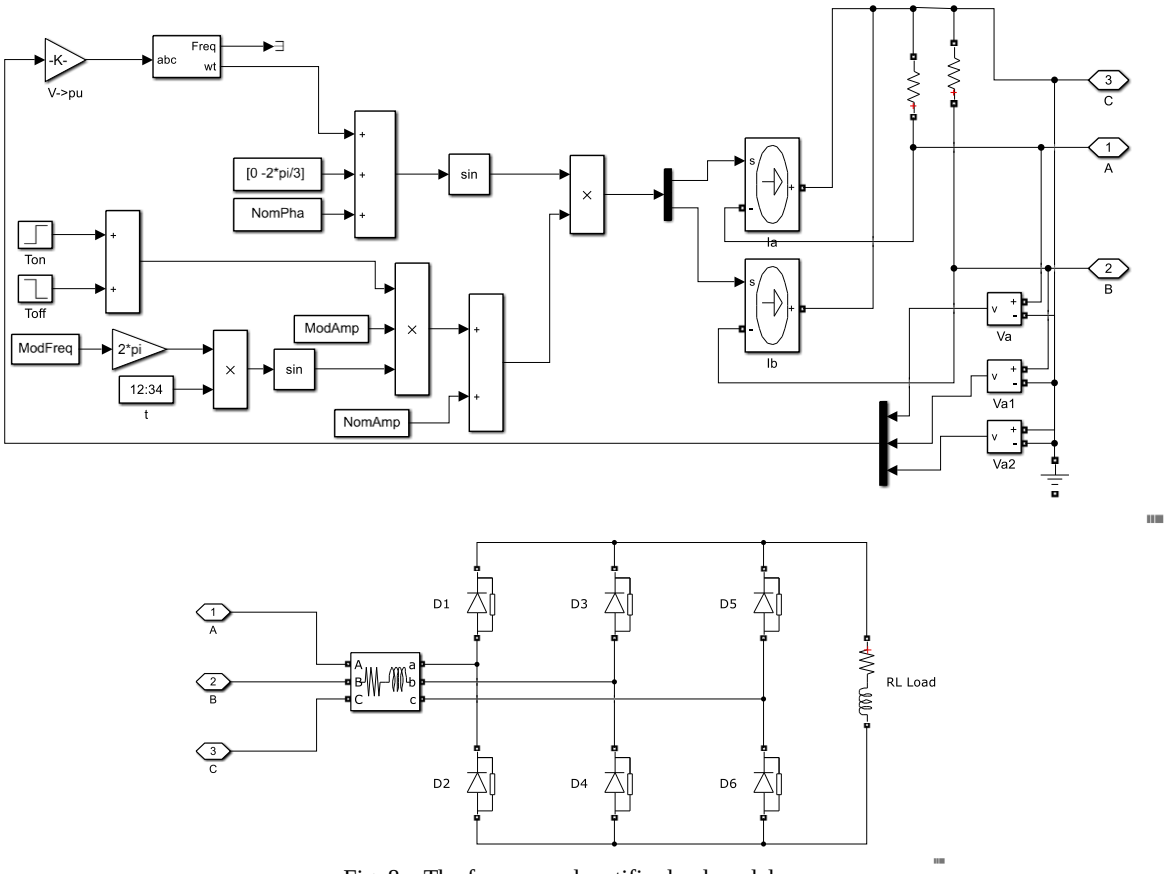


Fig. 8 – The furnace and rectifier load models.

Table 3

The nominal parameters of three-phase rectifier and three-phase electric arc furnace

Three-phase rectifier load				Three-phase electric arc furnace load				PV panel			
Load resistance	Load inductance	Snubber resistance	Snubber capacitance	Furnace current	Power factor	Modulation amplitude	Modulation frequency	Nominal voltage	Maximum power	Maximum voltage	Maximum current
60 Ω	20 mH	500 Ω	0.25 μF	10 A	0.9	7 A	200 Hz	12 V	250 W	35.5 V	6.77 A

5.1. Three-phase rectifier based nonlinear load

In this section, a three-phase rectifier based nonlinear load is considered to provide a harmonic current. To purify the power system current from the harmonic current caused by this nonlinear load, both active power filters have been evaluated here. It is considered that this nonlinear load imposes the current disturbances to the power system. Both filters have injected their compensation currents to eliminate current harmonics. Their relevant simulation results are presented in Fig. 9 and Fig. 10. As can be seen, ASHC-MLI based SHAPF can better purify power system current by injecting an accurate compensation current than the conventional active power filter. Since the proposed inverter provides 17-level quasi-sinusoidal voltage, the compensation process is more smoothly performed than conventional inverter.

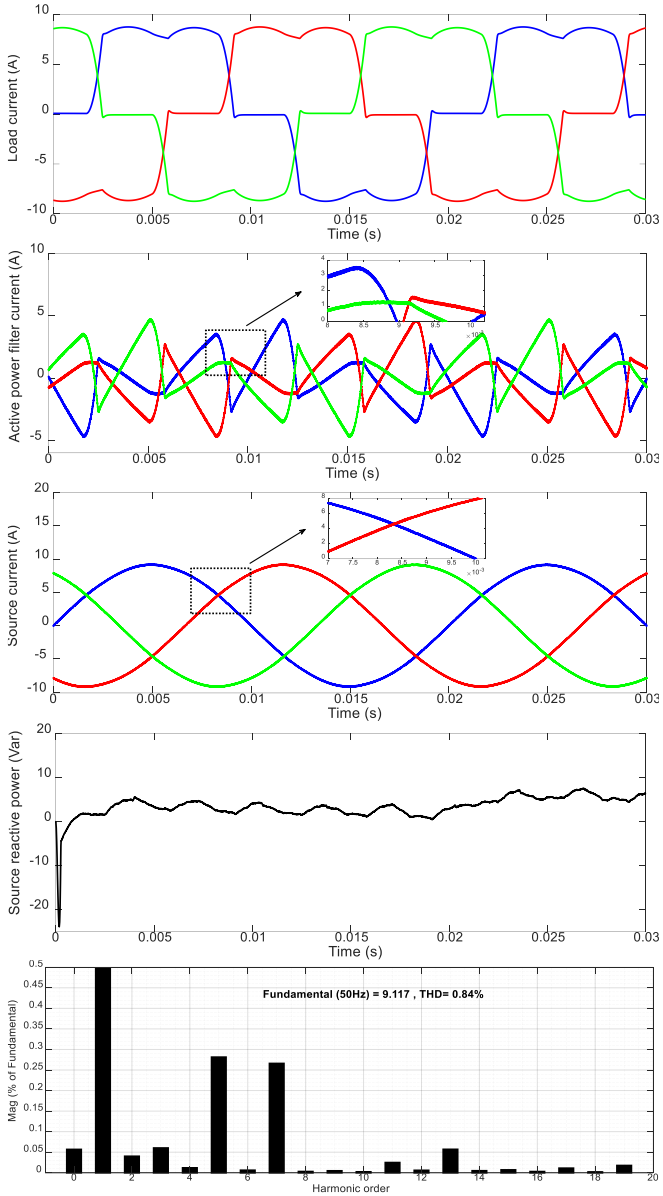


Fig. 9 – Power system responses with presence of ASHC-MLI based SHAPF: a) load current; b) SHAPF current; c) source current; d) source reactive power; e) FFT spectrum of the compensated current.

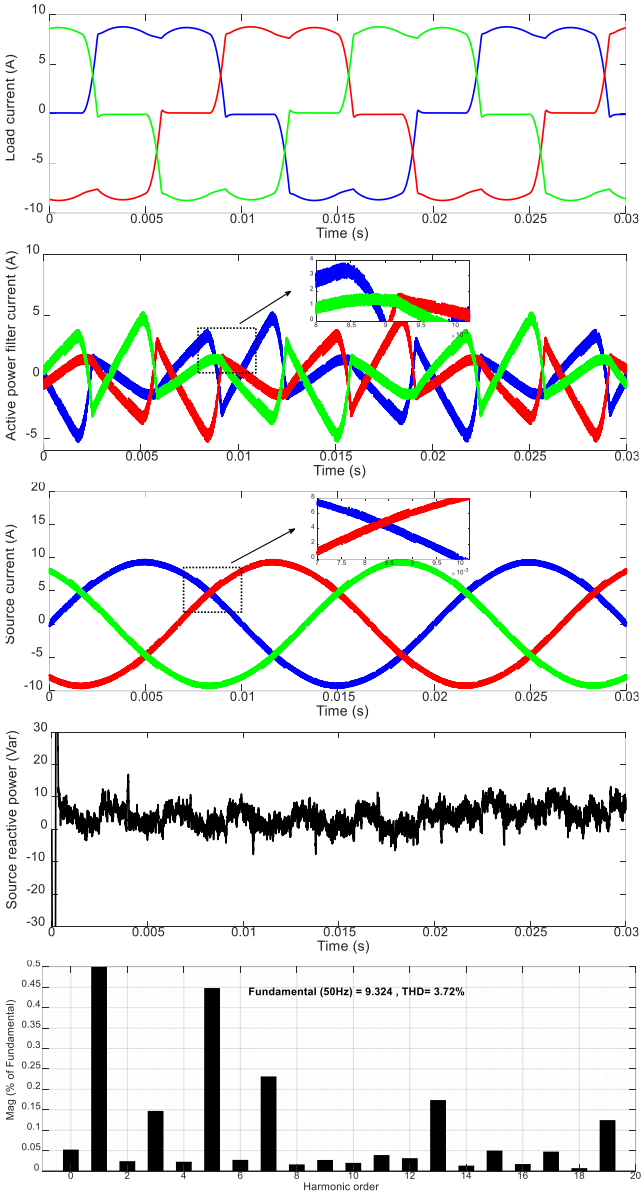


Fig. 10 – Power system responses with presence of conventional inverter based SHAPF: a) load current; b) SHAPF current; c) source current; d) source reactive power; e) FFT spectrum of the compensated current

5.2. Three-phase electric arc furnace load

The electric arc furnace is a furnace which melts the metals via electric arc. Due to its nonlinear and time-variant nature, great current fluctuations i.e. excessive current harmonic components have been released which must be eliminated. The proposed active filter with high-level production can be undertaken as a good alternative to compensate the relevant current harmonics. Hence, the electric arc furnace load enters in the load system. Same the previous section, both filters have injected their compensation currents to present their harmonic elimination capability. The simulation results under this disturbance are presented in Fig. 11 and Fig. 12. As expected, ASHC-MLI based SHAPF has more accurately compensated the current harmonics than the conventional active power filter. FFT and THD of the compensated current have clearly confirmed its harmonic elimination performance.

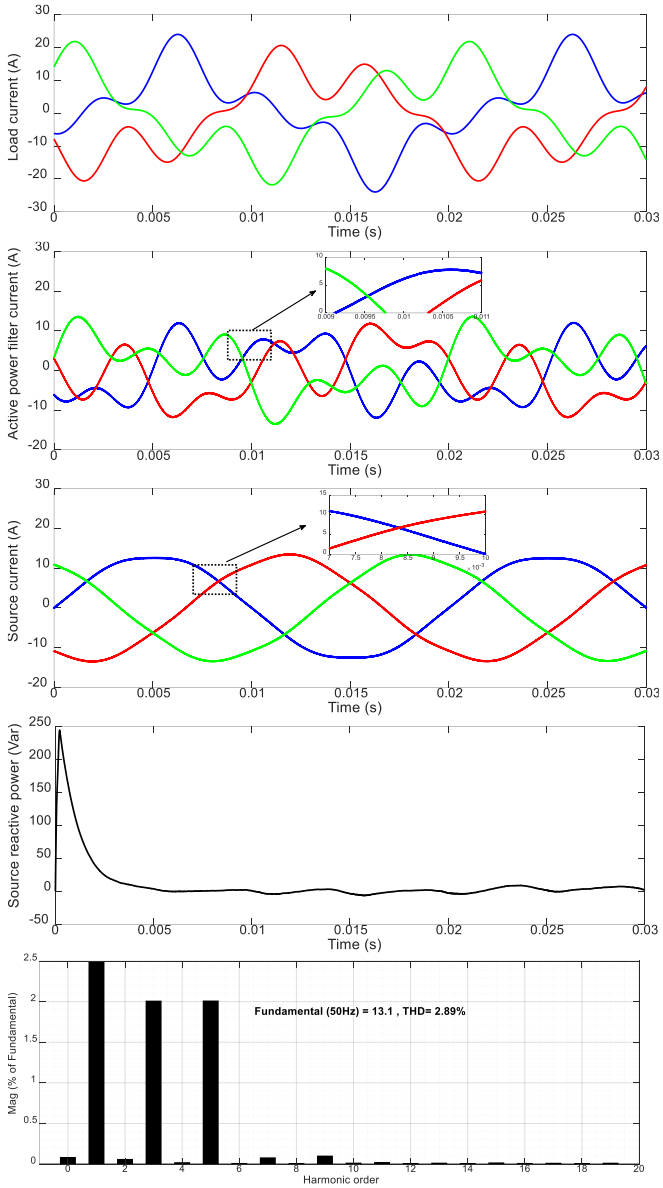


Fig. 11 – Power system responses with presence of ASHC-MLI based SHAPF: a) load current; b) SHAPF current; c) source current; d) source reactive power; e) FFT spectrum of the compensated current.

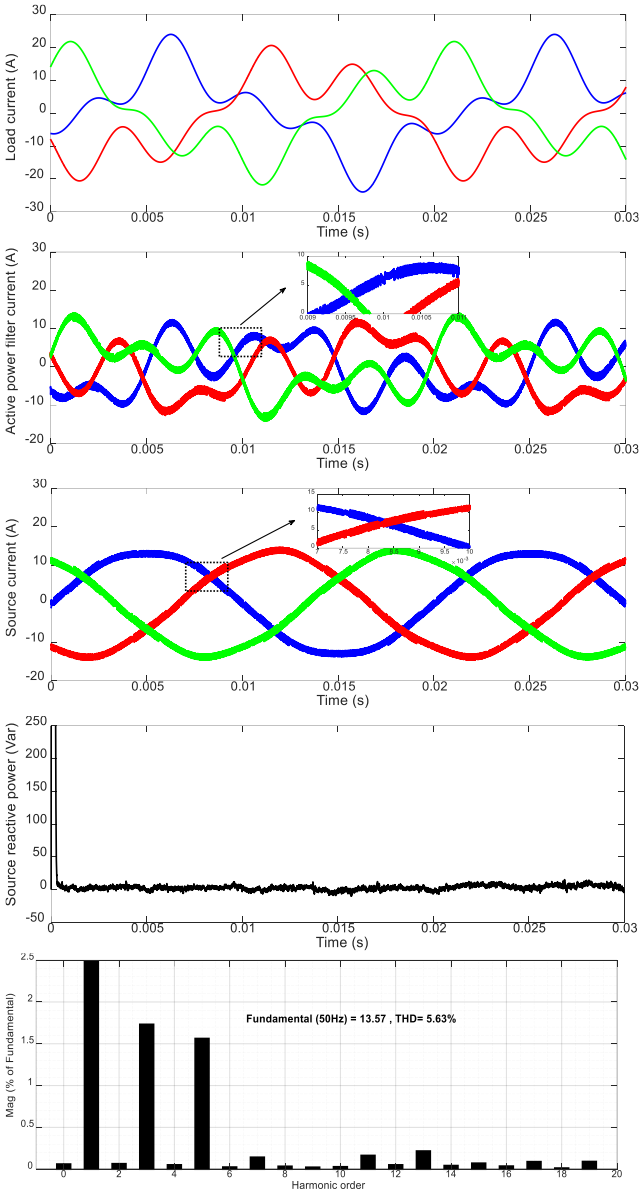


Fig. 12 – Power system responses with presence of conventional inverter based SHAPF: a) load current; b) SHAPF current; c) source current; d) source reactive power; e) FFT spectrum of the compensated current.

6. CONCLUSION

In this paper, a new asymmetric/symmetric half-cascaded multilevel inverter for active power filter is proposed for accurate compensation of current harmonics in distribution system. Since this proposed inverter requires a small number of switches to produce a high number of levels, it becomes very cost-effective and efficient. The level-generation capability of the proposed inverter, it has been compared with the prominent and inventive multilevel inverters in both asymmetric and symmetric statuses that the comparison results validate it. PV-based DC voltage source due to long-term energy generation and its eco-friendly nature, it has been integrated with battery energy storage to attain a constant and continuous DC voltage source of the proposed inverter. The proposed ASHC-MLI based SHAPF can accurately compensate the current harmonics with low THD. Also, its harmonic elimination capability has been compared with the SHAPF based on an inventive multilevel inverter that the relevant results have validated its performance.

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